AAT2120

SwitchReg™

500mA Low Noise Step-Down Converter

General Description

The AAT2120 SwitchReg is a 1.8MHz step-down converter with an input voltage range of 2.7V to 5.5V and output as low as 0.6V. Its low supply current, small size, and high switching frequency make the AAT2120 the ideal choice for portable applications.

The AAT2120 delivers up to 500mA of load current, while maintaining a low 45µA no load quiescent current. The 1.8MHz switching frequency minimizes the size of external components, while keeping switching losses low. The AAT2120 feedback and control delivers excellent load regulation and transient response with a small output inductor and capacitor.

The AAT2120 maintains high efficiency throughout the load range. The AAT2120's unique architecture produces reduced ripple and spectral noise. Over-temperature and short-circuit protection safeguard the AAT2120 and system components from damage.

The AAT2120 is available in a Pb-free, 8-pin, 2x2mm STDFN package and is rated over the -40°C to +85°C temperature range.

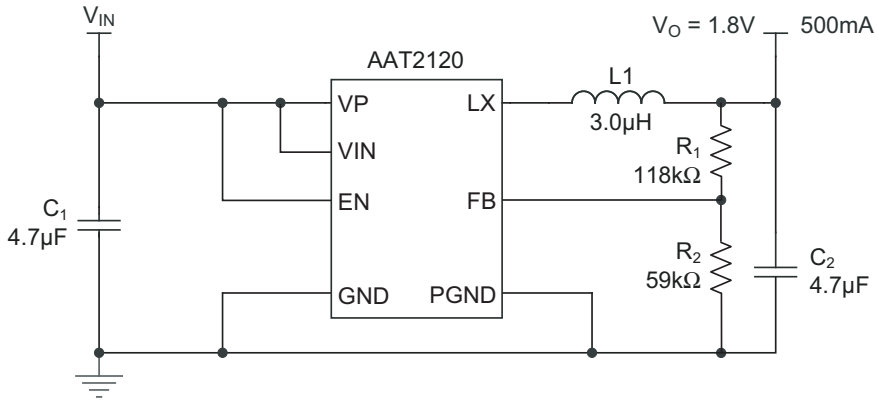
Features

- V_{IN} Range: 2.7V to 5.5V
- V_{OUT} Range: 0.6V to V_{IN}
- Up to 500mA Output Current
- Up to 96% Efficiency
- Low Noise Light Load Mode
- 45µA Typical Quiescent Current
- 1.8MHz Switching Frequency
- Soft-Start Control
- Over-Temperature and Current Limit Protection
- 100% Duty Cycle Low-Dropout Operation
- <1µA Shutdown Current
- Small External Components
- Ultra-Small STDFN22-8 Package
- Temperature Range: -40°C to +85°C

Applications

- Bluetooth® Headsets
- Cellular Phones
- Digital Cameras
- Handheld Instruments
- Micro Hard Disk Drive
- Portable Music Players
- USB Devices

Typical Application

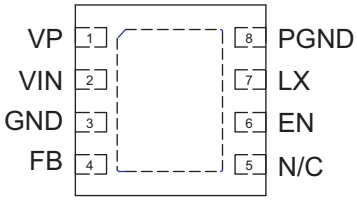


Pin Descriptions

Pin #	Symbol	Function
1	VP	Input power pin; connected to the source of the P-channel MOSFET. Connect to the input capacitor.
2	VIN	Input bias voltage for the converter.
3	GND	Non-power signal ground pin.
4	FB	Feedback input pin. Connect this pin to an external resistive divider for adjustable output.
5	N/C	No connect.
6	EN	Enable pin. A logic high enables normal operation. A logic low shuts down the converter.
7	LX	Switching node. Connect the inductor to this pin. It is connected internally to the drain of both high- and low-side MOSFETs.
8	PGND	Input power return pin; connected to the source of the N-channel MOSFET. Connect to the output and input capacitor return.
EP		Exposed paddle (bottom); connect to ground directly beneath the package.

Pin Configuration

STDFN22-8
(Top View)



Absolute Maximum Ratings[1]

Symbol	Description	Value	Units
V_{IN}	Input Voltage and Bias Power to GND	6.0	V
V_{LX}	LX to GND	-0.3 to V_{IN} + 0.3	V
V_{OUT}	FB to GND	-0.3 to V_{IN} + 0.3	V
V_{EN}	EN to GND	-0.3 to 6.0	V
T_J	Operating Junction Temperature Range	-40 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	300	°C

Thermal Information

Symbol	Description	Value	Units
P_D	Maximum Power Dissipation (STDFN22-8)	2	W
θ_{JA}	Thermal Resistance[2] (STDFN22-8)	50	°C/W

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum Rating should be applied at any one time.
2. Mounted on an FR4 board.

Electrical Characteristics[1]

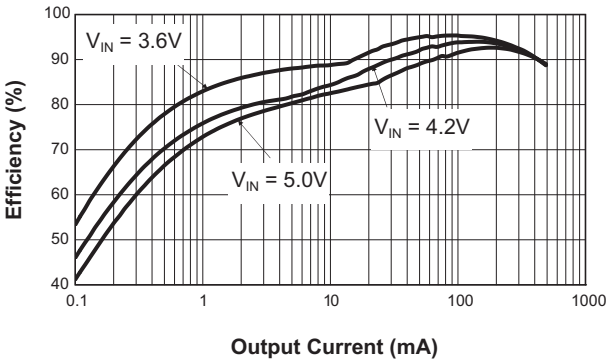
V_{IN} = 3.6V, T_A = -40°C to +85°C, unless otherwise noted; typical values are T_A = 25°C.

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{IN}	Input Voltage		2.7		5.5	V
V_{UVLO}	UVLO Threshold	V_{IN} Rising			2.3	V
		Hysteresis		70		mV
		V_{IN} Falling	1.4			V
V_{OUT}	Output Voltage Tolerance[2]	I_{OUT} = 0 to 500mA, V_{IN} = 2.7V to 5.5V	-3.0		3.0	%
V_{OUT}	Output Voltage Range		0.6		V_{IN}	V
I_Q	Quiescent Current	No Load		45	85	µA
I_{SHDN}	Shutdown Current	EN = GND			1.0	µA
I_{LIM}	P-Channel Current Limit			700		mA
$R_{DS(ON)H}$	High-Side Switch On Resistance			0.59		Ω
$R_{DS(ON)L}$	Low-Side Switch On Resistance			0.42		Ω
$\Delta V_{Linereg}/\Delta V_{IN}$	Line Regulation	V_{IN} = 2.7V to 5.5V		0.2		%/V
V_{FB}	Feedback Threshold Voltage Accuracy	V_{IN} = 3.6V	0.591	0.600	0.609	V
I_{FB}	FB Leakage Current	V_{OUT} = 1.0V			0.2	µA
F_{OSC}	Oscillator Frequency			1.8		MHz
T_S	Startup Time	From Enable to Output Regulation		100		µs
T_{SD}	Over-Temperature Shutdown Threshold			105		°C
T_{HYS}	Over-Temperature Shutdown Hysteresis			15		°C
$V_{EN(L)}$	Enable Threshold Low				0.6	V
$V_{EN(H)}$	Enable Threshold High		1.4			V
I_{EN}	Input Low Current	V_{IN} = V_{EN} = 5.5V	-1.0		1.0	µA

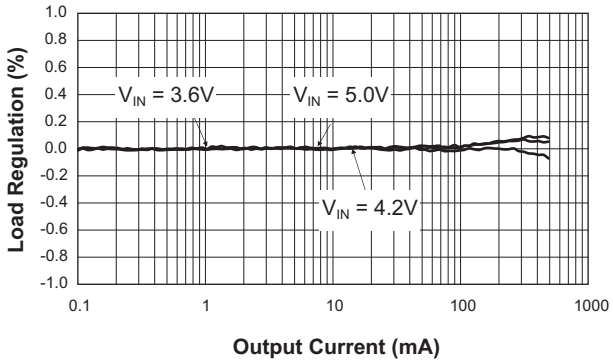
1. The AAT2120 is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range and is assured by design, characterization, and correlation with statistical process controls.
2. Output voltage tolerance is independent of feedback resistor network accuracy.

Typical Characteristics

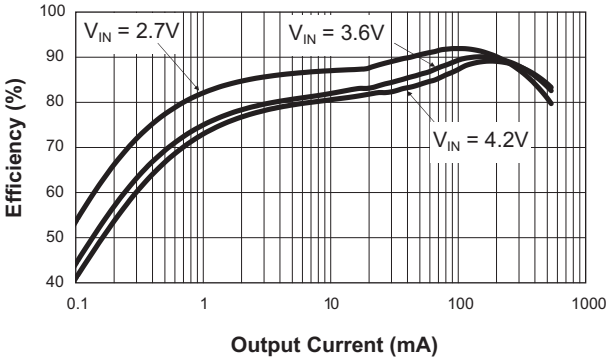
Efficiency vs. Load
(V_{OUT} = 3.0V; L = 4.7µH)



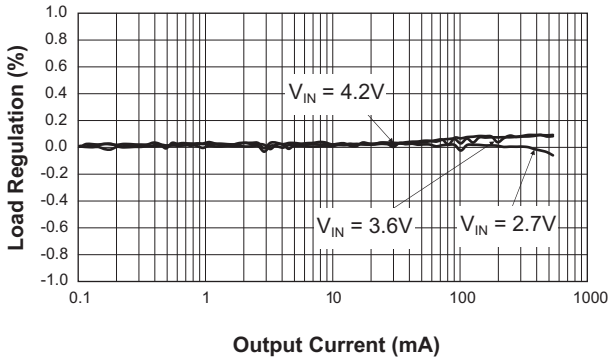
Load Regulation
(V_{OUT} = 3.0V; L = 4.7µH)



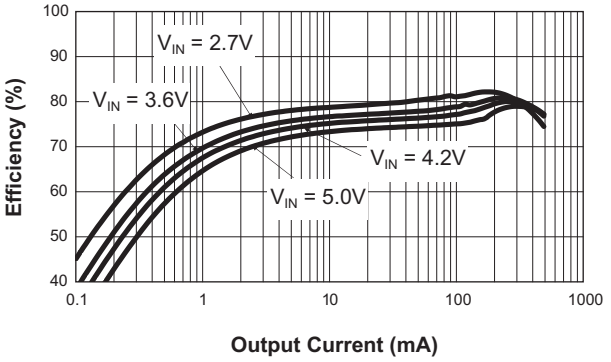
Efficiency vs. Load
(V_{OUT} = 1.8V; L = 3.3µH)



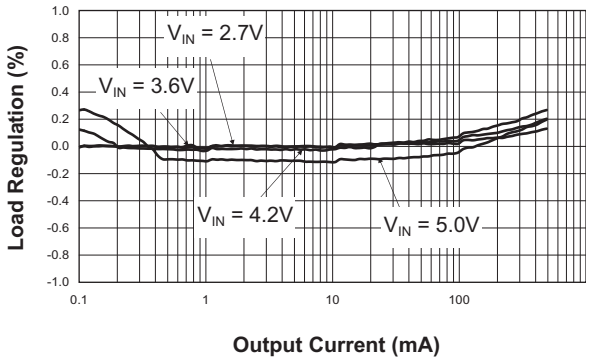
Load Regulation
(V_{OUT} = 1.8V; L = 3.3µH)



Efficiency vs. Load
(V_{OUT} = 1.2V; L = 1.5µH)

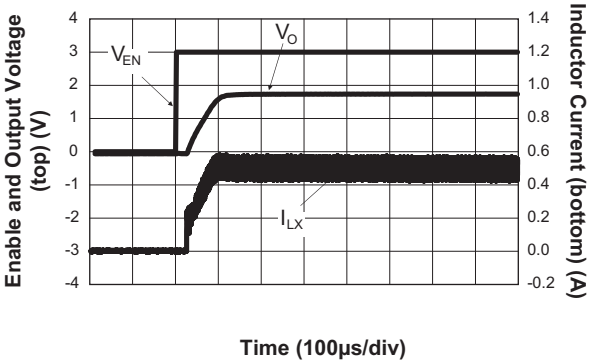


Load Regulation
(V_{OUT} = 1.2V; L = 1.5µH)

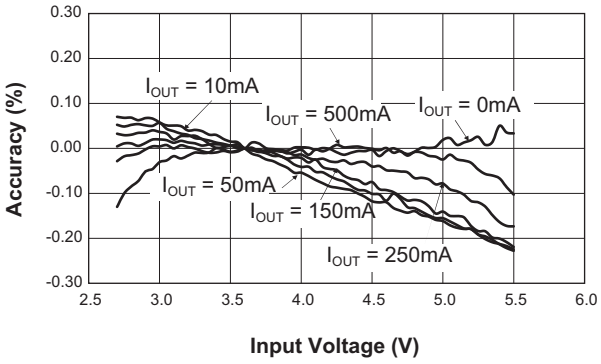


Typical Characteristics

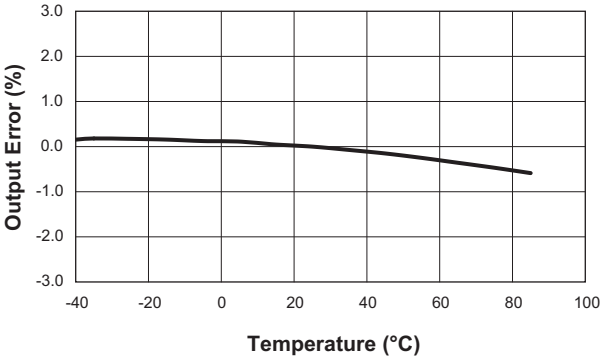
Soft Start
(V_{IN} = 3.6V; V_{OUT} = 1.8V; 500mA)



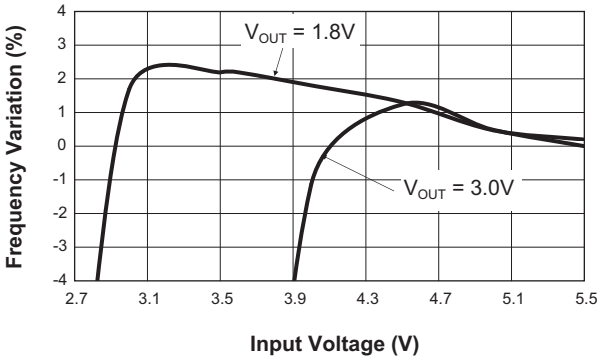
Line Regulation
(V_{OUT} = 1.8V)



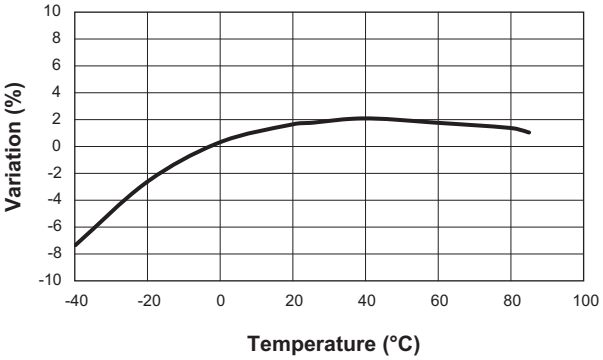
Output Voltage Error vs. Temperature
(V_{IN} = 3.6V; V_{OUT} = 1.8V; I_{OUT} = 500mA)



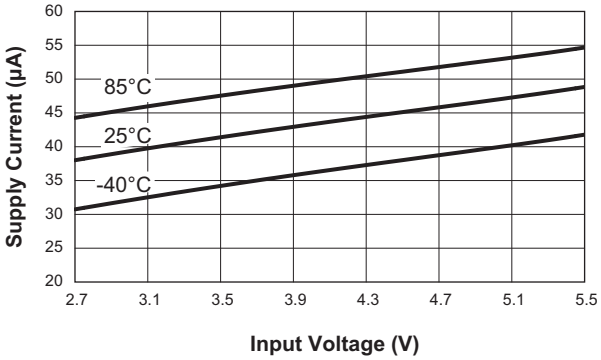
Frequency Variation vs. Input Voltage



Switching Frequency Variation vs. Temperature
(V_{IN} = 3.6V; V_{OUT} = 1.8V)

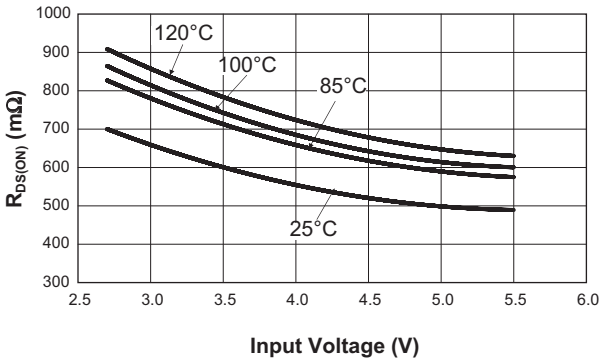


No Load Quiescent Current vs. Input Voltage

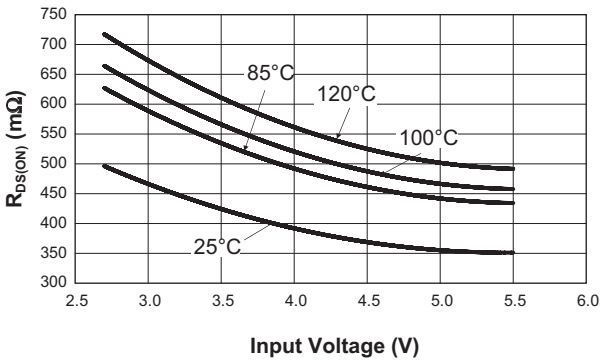


Typical Characteristics

P-Channel $R_{DS(ON)}$ vs. Input Voltage

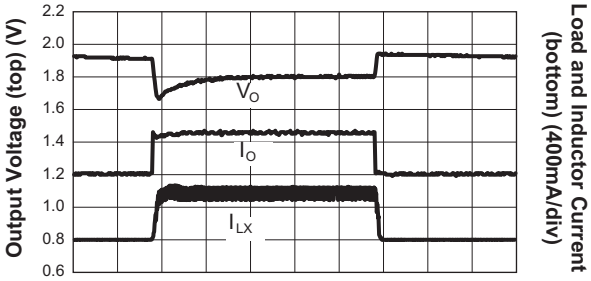


N-Channel $R_{DS(ON)}$ vs. Input Voltage



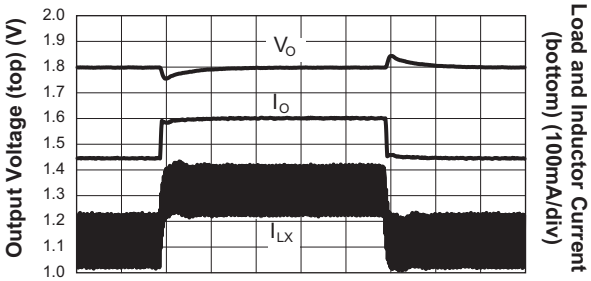
Load Transient Response

(1mA to 500mA; V_{IN} = 3.6V; V_{OUT} = 1.8V; C_{OUT} = 4.7µF; C_{FF} = 100pF)



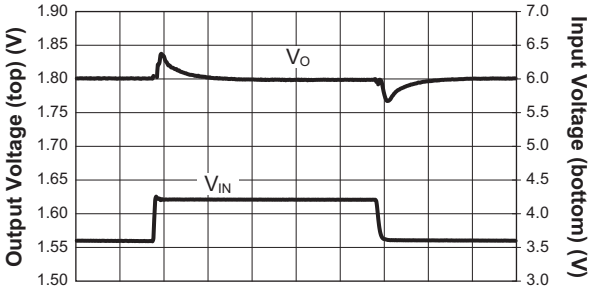
Load Transient Response

(350mA to 500mA; V_{IN} = 3.6V; V_{OUT} = 1.8V; C_{OUT} = 4.7µF; C_{FF} = 100pF)



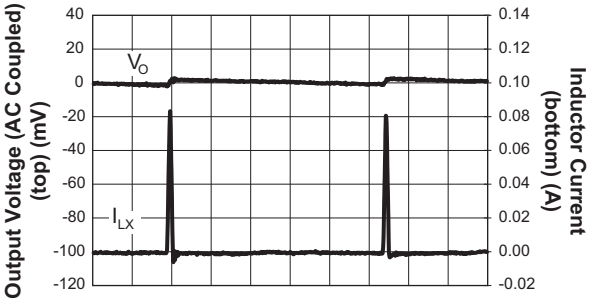
Line Response

(V_{OUT} = 1.8V @ 500mA)



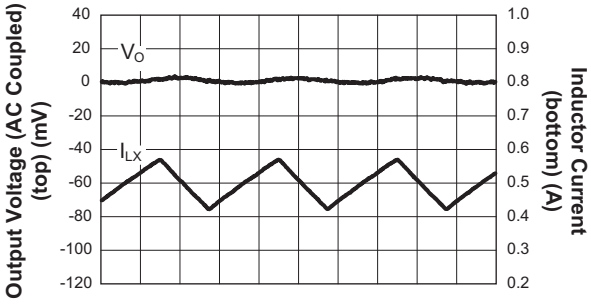
Typical Characteristics

Output Ripple
(V_{IN} = 3.6V; V_{OUT} = 1.8V; I_{OUT} = 1mA)



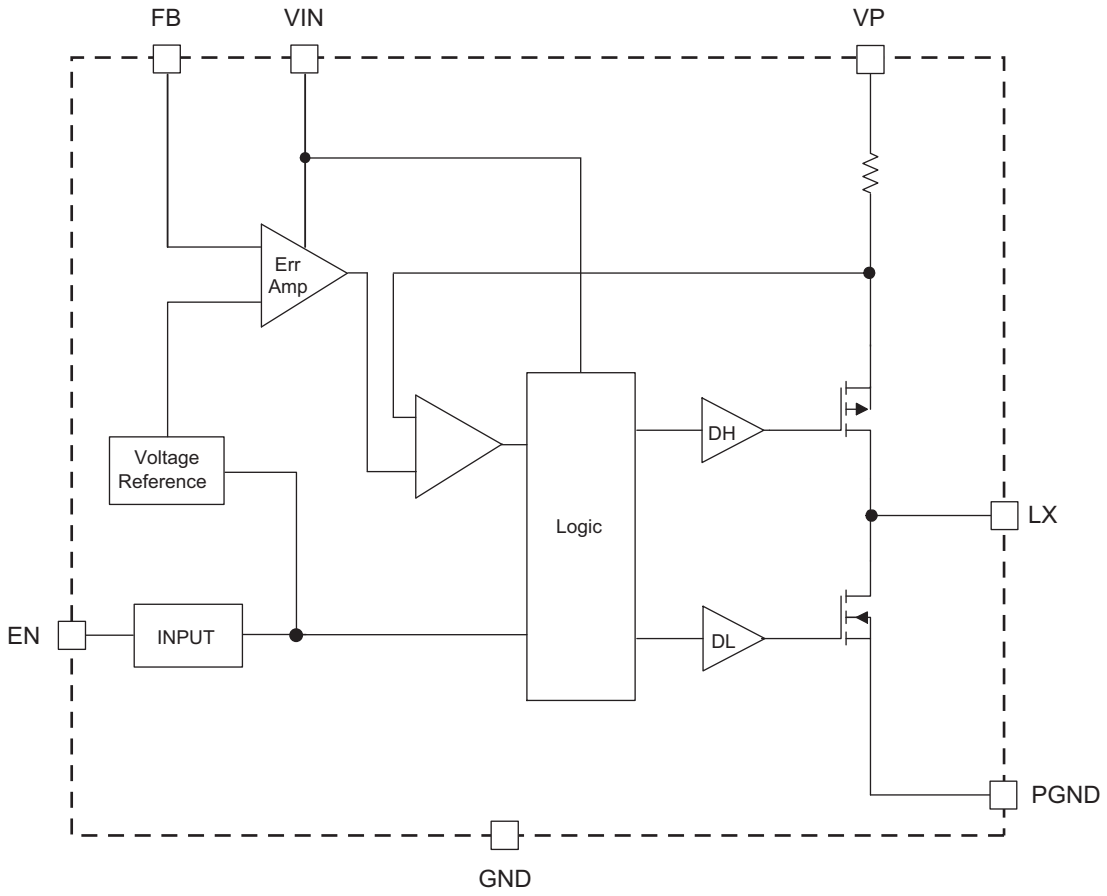
Time (2µs/div)

Output Ripple
(V_{IN} = 3.6V; V_{OUT} = 1.8V; I_{OUT} = 500mA)



Time (200ns/div)

Functional Block Diagram



Functional Description

The AAT2120 is a high performance 500mA, 1.8MHz monolithic step-down converter designed to operate with an input voltage range of 2.7V to 5.5V. The converter operates at 1.8MHz, which minimizes the size of external components. Typical values are 3.3µH for the output inductor and 4.7µF for the ceramic output capacitor.

The device is designed to operate with an output voltage as low as 0.6V. Power devices are sized for 500mA current capability while maintaining over 90% efficiency at full load. Low current efficiency is maintained at greater than 80% down to 1mA of load current.

At dropout, the converter duty cycle increases to 100% and the output voltage tracks the input voltage minus the $R_{DS(ON)}$ drop of the P-channel highside MOSFET.

A high-DC gain error amplifier with internal compensation controls the output. It provides excellent transient response and load/line regulation. Soft start eliminates any output voltage overshoot when the enable or the input voltage is applied.

Control Loop

The AAT2120 is a 500mA current mode step-down converter. The current through the P-channel MOSFET (high side) is sensed for current loop control, as well as short-

circuit and overload protection. A fixed slope compensation signal is added to the sensed current to maintain stability for duty cycles greater than 50%. The peak current mode loop appears as a voltage-programmed current source in parallel with the output capacitor.

The output of the voltage error amplifier programs the current mode loop for the necessary peak switch current to force a constant output voltage for all load and line conditions. Internal loop compensation terminates the transconductance voltage error amplifier output. The error amplifier reference is fixed at 0.6V.

Soft Start / Enable

Soft start increases the inductor current limit point in discrete steps when the input voltage or enable input is applied. It limits the current surge seen at the input and eliminates output voltage overshoot. When pulled low, the enable input forces the AAT2120 into a low-power, non-switching state. The total input current during shutdown is less than 1µA.

Current Limit and Over-Temperature Protection

For overload conditions, the peak input current is limited. As load impedance decreases and the output voltage falls closer to zero, more power is dissipated internally, raising the device temperature. Thermal protection completely disables switching when internal dissipation becomes excessive, protecting the device from damage. The junction over-temperature threshold is 105°C with 15°C of hysteresis.

Under-Voltage Lockout

Internal bias of all circuits is controlled via the V_{IN} power. Under-voltage lockout (UVLO) guarantees sufficient V_{IN} bias and proper operation of all internal circuits prior to activation.

Applications Information

Inductor Selection

The step-down converter uses peak current mode control with slope compensation to maintain stability for duty cycles greater than 50%. The output inductor value must be selected so the inductor current down slope meets the internal slope compensation requirements. The internal slope compensation for the adjustable and low-voltage fixed versions of the AAT2120 is 0.45A/µs. This equates to a slope compensation that is 75% of the inductor current down slope for a 1.8V output and 3.0µH inductor.

$$m = \frac{0.75 \cdot V_O}{L} = \frac{0.75 \cdot 1.8V}{3.0\mu H} = 0.45\,\frac{A}{\mu s}$$

This is the internal slope compensation for the AAT2120. When externally programming to 3.0V, the calculated inductance is 5.0µH.

$$L = \frac{0.75 \cdot V_O}{m} = \frac{0.75 \cdot V_O}{0.45A\,\frac{A}{\mu s}} \approx 1.67\,\frac{\mu s}{A} \cdot V_O$$

$$= 1.67\,\frac{\mu s}{A} \cdot 3.0V = 5.0\mu H$$

In this case, a standard 4.7µH value is selected.

For most designs, the AAT2120 operates with an inductor value of 1µH to 4.7µH. Table 1 displays inductor values for the AAT2120 with different output voltage options.

Manufacturer's specifications list both the inductor DC current rating, which is a thermal limitation, and the peak current rating, which is determined by the saturation characteristics. The inductor should not show any appreciable saturation under normal load conditions. Some inductors may meet the peak and average current ratings yet result in excessive losses due to a high DCR. Always consider the losses associated with the DCR and its effect on the total converter efficiency when selecting an inductor.

Output Voltage (V)	L1 (µH)
1.0	1.5
1.2	2.2
1.5	2.7
1.8	3.0
2.5	3.9
3.0	4.7
3.3	5.6

Table 1: Inductor Values.

The 3.0µH CDRH2D09 series inductor selected from Sumida has a 150mΩ DCR and a 470mA DC current rating. At full load, the inductor DC loss is 9.375mW which gives a 2.08% loss in efficiency for a 250mA, 1.8V output.

Input Capacitor

Select a 4.7µF to 10µF X7R or X5R ceramic capacitor for the input. To estimate the required input capacitor size, determine the acceptable input ripple level (V_{PP}) and solve for C_{IN}. The calculated value varies with input voltage and is a maximum when V_{IN} is double the output voltage.

$$C_{IN} = \frac{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}{\left(\frac{V_{PP}}{I_O} - ESR\right) \cdot F_S}$$

$$\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right) = \frac{1}{4} \text{ for } V_{IN} = 2 \cdot V_O$$

$$C_{IN(MIN)} = \frac{1}{\left(\frac{V_{PP}}{I_O} - ESR\right) \cdot 4 \cdot F_S}$$

Always examine the ceramic capacitor DC voltage coefficient characteristics when selecting the proper value. For example, the capacitance of a 10µF, 6.3V, X5R ceramic capacitor with 5.0V DC applied is actually about 6µF.

The maximum input capacitor RMS current is:

$$I_{RMS} = I_O \cdot \sqrt{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}$$

The input capacitor RMS ripple current varies with the input and output voltage and will always be less than or equal to half of the total DC load current.

$$\sqrt{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)} = \sqrt{D \cdot (1 - D)} = \sqrt{0.5^2} = \frac{1}{2}$$

for $V_{IN} = 2 \cdot V_O$

$$I_{RMS(MAX)} = \frac{I_O}{2}$$

The term $\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)$ appears in both the input voltage ripple and input capacitor RMS current equations and is a maximum when V_O is twice V_{IN}. This is why the input voltage ripple and the input capacitor RMS current ripple are a maximum at 50% duty cycle.

The input capacitor provides a low impedance loop for the edges of pulsed current drawn by the AAT2120. Low ESR/ESL X7R and X5R ceramic capacitors are ideal for this function. To minimize stray inductance, the capacitor should be placed as closely as possible to the IC. This keeps the high frequency content of the input current localized, minimizing EMI and input voltage ripple.

The proper placement of the input capacitor (C1) can be seen in the evaluation board layout in Figure 2.

A laboratory test set-up typically consists of two long wires running from the bench power supply to the evaluation board input voltage pins. The inductance of these wires, along with the low-ESR ceramic input capacitor, can create a high Q network that may affect converter performance. This problem often becomes apparent in the form of excessive ringing in the output voltage during load transients. Errors in the loop phase and gain measurements can also result.

Since the inductance of a short PCB trace feeding the input voltage is significantly lower than the power leads from the bench power supply, most applications do not exhibit this problem.

In applications where the input power source lead inductance cannot be reduced to a level that does not affect the converter performance, a high ESR tantalum or aluminum electrolytic should be placed in parallel with the low ESR, ESL bypass ceramic. This dampens the high Q network and stabilizes the system.

Output Capacitor

The output capacitor limits the output ripple and provides holdup during large load transitions. A 4.7µF to 10µF X5R or X7R ceramic capacitor typically provides sufficient bulk capacitance to stabilize the output during large load transitions and has the ESR and ESL characteristics necessary for low output ripple. For enhanced

transient response and low temperature operation application, a 10µF (X5R, X7R) ceramic capacitor is recommended to stabilize extreme pulsed load conditions.

The output voltage droop due to a load transient is dominated by the capacitance of the ceramic output capacitor. During a step increase in load current, the ceramic output capacitor alone supplies the load current until the loop responds. Within two or three switching cycles, the loop responds and the inductor current increases to match the load current demand. The relationship of the output voltage droop during the three switching cycles to the output capacitance can be estimated by:

$$C_{OUT} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot F_S}$$

Once the average inductor current increases to the DC load level, the output voltage recovers. The above equation establishes a limit on the minimum value for the output capacitor with respect to load transients.

The internal voltage loop compensation also limits the minimum output capacitor value to 4.7µF. This is due to its effect on the loop crossover frequency (bandwidth), phase margin, and gain margin. Increased output capacitance will reduce the crossover frequency with greater phase margin.

The maximum output capacitor RMS ripple current is given by:

$$I_{RMS(MAX)} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{V_{OUT} \cdot (V_{IN(MAX)} - V_{OUT})}{L \cdot F_S \cdot V_{IN(MAX)}}$$

Dissipation due to the RMS current in the ceramic output capacitor ESR is typically minimal, resulting in less than a few degrees rise in hot-spot temperature.

Adjustable Output Resistor Selection

Resistors R1 and R2 of Figure 1 program the output to regulate at a voltage higher than 0.6V. To limit the bias current required for the external feedback resistor string while maintaining good noise immunity, the suggested value for R2 is 59kΩ. Decreased resistor values are necessary to maintain noise immunity on the FB pin, resulting in increased quiescent current. Table 2 summarizes the resistor values for various output voltages.

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \cdot R2 = \left(\frac{3.3V}{0.6V} - 1\right) \cdot 59k\Omega = 267k\Omega$$

With enhanced transient response for extreme pulsed load application, an external feed-forward capacitor, (C3 in Figure 1), can be added.

V_{OUT} (V)	R2 = 59kΩ R1 (kΩ)	R2 = 221kΩ R1 (kΩ)
0.8	19.6	75
0.9	29.4	113
1.0	39.2	150
1.1	49.9	187
1.2	59.0	221
1.3	68.1	261
1.4	78.7	301
1.5	88.7	332
1.8	118	442
1.85	124	464
2.0	137	523
2.5	187	715
3.3	267	1000

Table 2: Adjustable Resistor Values for Step-Down Converter.

Thermal Calculations

There are three types of losses associated with the AAT2120 step-down converter: switching losses, conduction losses, and quiescent current losses. Conduction losses are associated with the $R_{DS(ON)}$ characteristics of the power output switching devices. Switching losses are dominated by the gate charge of the power output switching devices. At full load, assuming continuous conduction mode (CCM), a simplified form of the losses is given by:

$$P_{TOTAL} = \frac{I_O^2 \cdot (R_{DS(ON)H} \cdot V_O + R_{DS(ON)L} \cdot [V_{IN} - V_O])}{V_{IN}}$$

$$+ (t_{sw} \cdot F_S \cdot I_O + I_Q) \cdot V_{IN}$$

I_Q is the step-down converter quiescent current. The term t_{sw} is used to estimate the full load step-down converter switching losses.

For the condition where the step-down converter is in dropout at 100% duty cycle, the total device dissipation reduces to:

$$P_{TOTAL} = I_O^2 \cdot R_{DSON(H)} + I_Q \cdot V_{IN}$$

Since $R_{DS(ON)}$, quiescent current, and switching losses all vary with input voltage, the total losses should be investigated over the complete input voltage range.

Given the total losses, the maximum junction temperature can be derived from the θ_{JA} for the STDFN22-8 package which is 50°C/W.

$$T_{J(MAX)} = P_{TOTAL} \cdot \Theta_{JA} + T_{AMB}$$

Layout

The suggested PCB layout for the AAT2120 in an STDFN22-8 package is shown in Figures 2, 3, and 4. The following guidelines should be used to help ensure a proper layout.

1. The input capacitor (C1) should connect as closely as possible to VP (Pin 1), PGND (Pin 8), and GND (Pin 3)
2. C2 and L1 should be connected as closely as possible. The connection of L1 to the LX pin (Pin 7) should be as short as possible. Do not make the node small by using narrow trace. The trace should be kept wide, direct and short.
3. The feedback pin (Pin 4) should be separate from any power trace and connect as closely as possible to the load point. Sensing along a high-current load trace will degrade DC load regulation. Feedback resistors should be placed as closely as possible to the FB pin (Pin 4) to minimize the length of the high impedance feedback trace. If possible, they should also be placed away from the LX (switching node) and inductor to improve noise immunity.
4. The resistance of the trace from the load return to PGND (Pin 8) and GND (Pin 3) should be kept to a minimum. This will help to minimize any error in DC regulation due to differences in the potential of the internal signal ground and the power ground.
5. A high density, small footprint layout can be achieved using an inexpensive, miniature, non-shielded, high DCR inductor.

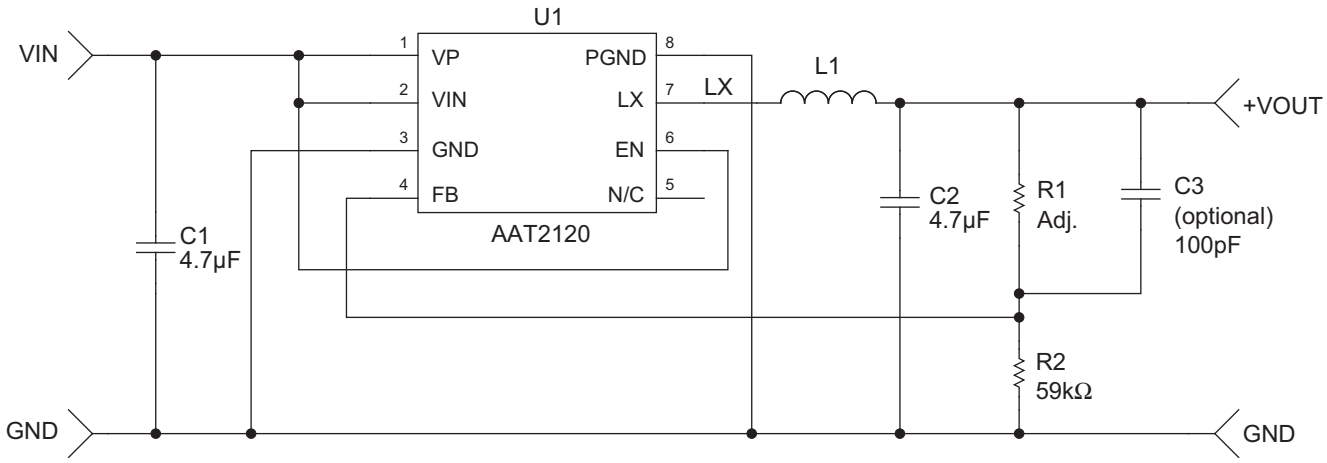


Figure 1: AAT2120 Schematic.

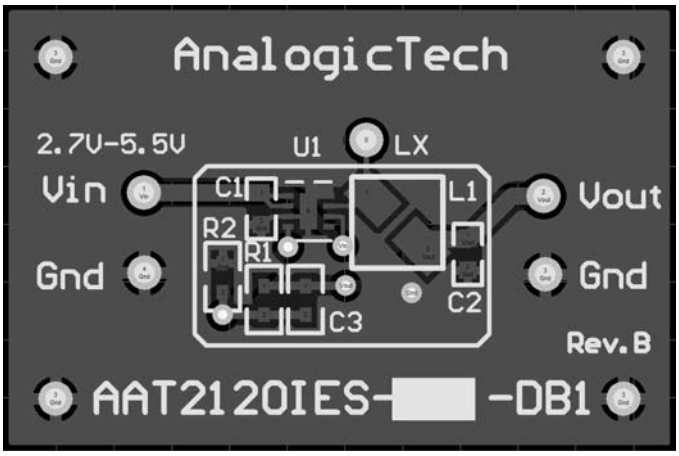


Figure 2: AAT2120 Evaluation Board Top Side Layout.

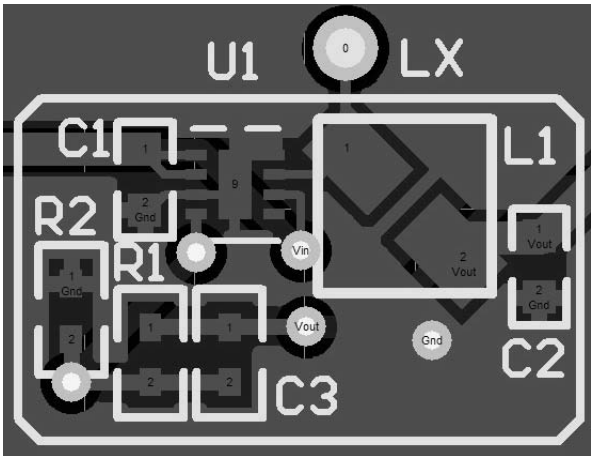


Figure 3: Exploded View of AAT2120 Evaluation Board Top Side Layout.

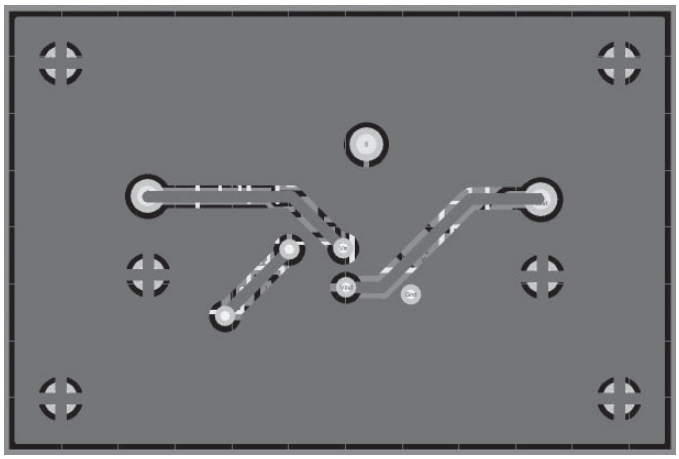


Figure 4: AAT2120 Evaluation Board Bottom Side Layout.

Step-Down Converter Design Example

Specifications

V_O = 1.8V @ 250mA, Pulsed Load ΔI_{LOAD} = 200mA
V_{IN} = 2.7V to 4.2V (3.6V nominal)
F_S = 1.8MHz
T_{AMB} = 85°C

1.8V Output Inductor

$$L1 = 1.67\,\frac{\mu s}{A} \cdot V_{O2} = 1.67\,\frac{\mu s}{A} \cdot 1.8V = 3\mu H$$ (use 3.0µH; see Table 1)

For Sumida inductor CDRH2D09-3R0, 3.0µH, DCR = 150mΩ.

$$\Delta I_{L1} = \frac{V_O}{L1 \cdot F_S} \cdot \left(1 - \frac{V_O}{V_{IN}}\right) = \frac{1.8V}{3.0\mu H \cdot 1.8MHz} \cdot \left(1 - \frac{1.8V}{4.2V}\right) = 190mA$$

$$I_{PKL1} = I_O + \frac{\Delta I_{L1}}{2} = 250mA + 95mA = 345mA$$

$$P_{L1} = I_O^2 \cdot DCR = 250mA^2 \cdot 150m\Omega = 9.375mW$$

1.8V Output Capacitor

V_{DROOP} = 0.1V

$$C_{OUT} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot F_S} = \frac{3 \cdot 0.2A}{0.1V \cdot 1.8MHz} = 3.3\mu F \text{ (use } 3.3\mu F)$$

$$I_{RMS} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{(V_O) \cdot (V_{IN(MAX)} - V_O)}{L1 \cdot F_S \cdot V_{IN(MAX)}} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{1.8V \cdot (4.2V - 1.8V)}{3.0\mu H \cdot 1.8MHz \cdot 4.2V} = 66mArms$$

$$P_{esr} = esr \cdot I_{RMS}^2 = 5m\Omega \cdot (66mA)^2 = 21.8\mu W$$

Input Capacitor

Input Ripple V_{PP} = 25mV

$$C_{IN} = \frac{1}{\left(\frac{V_{PP}}{I_O} - ESR\right) \cdot 4 \cdot F_S} = \frac{1}{\left(\frac{25mV}{0.2A} - 5m\Omega\right) \cdot 4 \cdot 1.8MHz} = 1.16\mu F \text{ (use } 4.7\mu F)$$

$$I_{RMS} = \frac{I_O}{2} = 0.1Arms$$

$$P = esr \cdot I_{RMS}^2 = 5m\Omega \cdot (0.1A)^2 = 0.05mW$$

AAT2120 Losses

$$P_{TOTAL} = \frac{I_O^2 \cdot (R_{DS(ON)H} \cdot V_O + R_{DS(ON)L} \cdot [V_{IN} - V_O])}{V_{IN}}$$

$$+ (t_{sw} \cdot F_S \cdot I_O + I_Q) \cdot V_{IN}$$

$$= \frac{0.2^2 \cdot (0.59\Omega \cdot 1.8V + 0.42\Omega \cdot [4.2V - 1.8V])}{4.2V}$$

$$+ (5ns \cdot 1.8MHz \cdot 0.2A + 45\mu A) \cdot 4.2V = 19.71mW$$

$$T_{J(MAX)} = T_{AMB} + \Theta_{JA} \cdot P_{LOSS} = 85°C + (50°C/W) \cdot 26.14mW = 86°C$$

Output Voltage V_{OUT} (V)	R2 = 59kΩ R1 (kΩ)	R2 = 221kΩ[1] R1 (kΩ)	L1 (µH)
0.62	—	—	1.5
0.8	19.6	75	1.5
0.9	29.4	113	1.5
1.0	39.2	150	1.5
1.1	49.9	187	1.5
1.2	59.0	221	1.5
1.3	68.1	261	1.5
1.4	78.7	301	2.2
1.5	88.7	332	2.7
1.8	118	442	3.0/3.3
1.85	124	464	3.0/3.3
2.0	137	523	3.0/3.3
2.5	187	715	3.9/4.2
3.3	267	1000	5.6

Table 3: Evaluation Board Component Values.

Manufacturer	Part Number	Inductance (µH)	Max DC Current (mA)	DCR (mΩ)	Size (mm) LxWxH	Type
Sumida	CDRH2D14-1R5	1.5	1800	50	3.0x3.0x1.55	Shielded
Sumida	CDRH2D14-2R2	2.2	1500	75	3.0x3.0x1.55	Shielded
Sumida	CDRH2D14-2R7	2.7	1350	85	3.0x3.0x1.55	Shielded
Sumida	CDRH2D14-3R3	3.3	1200	100	3.0x3.0x1.55	Shielded
Sumida	CDRH2D14-3R9	3.9	1100	110	3.0x3.0x1.55	Shielded
Sumida	CDRH2D14-4R7	4.7	1000	135	3.0x3.0x1.55	Shielded
Sumida	CDRH2D14-5R6	5.6	950	150	3.0x3.0x1.55	Shielded
Sumida	CDRH2D11-1R5	1.5	900	54	3.2x3.2x1.2	Shielded
Sumida	CDRH2D11-2R2	2.2	780	78	3.2x3.2x1.2	Shielded
Sumida	CDRH2D11-3R3	3.3	600	98	3.2x3.2x1.2	Shielded
Sumida	CDRH2D11-4R7	4.7	500	135	3.2x3.2x1.2	Shielded
Taiyo Yuden	NR3010	1.5	1200	80	3.0x3.0x1.0	Shielded
Taiyo Yuden	NR3010	2.2	1100	95	3.0x3.0x1.0	Shielded
Taiyo Yuden	NR3010	3.3	870	140	3.0x3.0x1.0	Shielded
Taiyo Yuden	NR3010	4.7	750	190	3.0x3.0x1.0	Shielded
FDK	MIPWT3226D-1R5	1.5	1200	90	3.2x2.6x0.8	Chip shielded
FDK	MIPWT3226D-2R2	2.2	1100	100	3.2x2.6x0.8	Chip shielded
FDK	MIPWT3226D-3R0	3	1000	120	3.2x2.6x0.8	Chip shielded
FDK	MIPWT3226D-4R2	4.2	900	140	3.2x2.6x0.8	Chip shielded

Table 4: Suggested Inductors and Suppliers.

Manufacturer	Part Number	Value (µF)	Voltage Rating	Temp. Co.	Case Size
Murata	GRM118R60J475KE19B	4.7	6.3	X5R	0603
Murata	GRM188R60J106ME47D	10	6.3	X5R	0603

Table 5: Surface Mount Capacitors.

1. For reduced quiescent current, R2 = 221kΩ.
2. R2 is opened, R1 is shorted.

Ordering Information

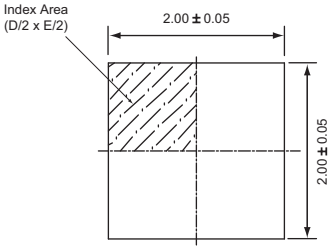
Output Voltage	Package	Marking[1]	Part Number (Tape and Reel)[2]
0.6V	STDFN22-8	YDXYY	**AAT2120IES-0.6-T1**

All AnalogicTech products are offered in Pb-free packaging. The term "Pb-free" means semiconductor products that are in compliance with current RoHS standards, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. For more information, please visit our website at http://www.analogictech.com/about/quality.aspx.

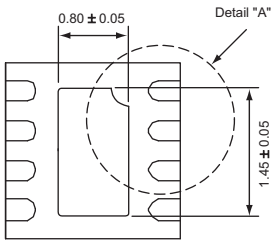
1. XYY = assembly and date code.
2. Sample stock is generally held on all part numbers listed in **BOLD**.

Package Information[1]

STDFN22-8

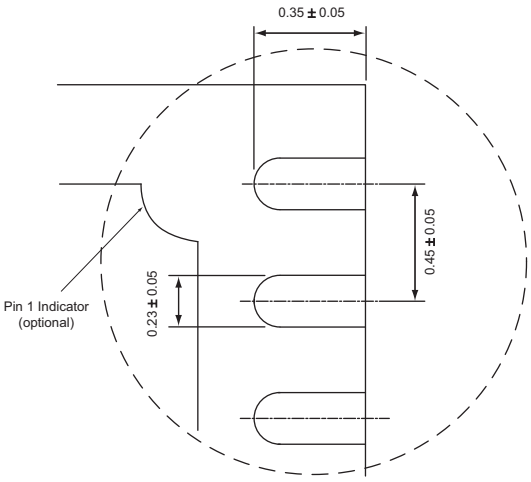


Top View



Bottom View

Side View



Detail "A"

All dimensions in millimeters.

1. The leadless package family, which includes QFN, TQFN, DFN, TDFN and STDFN, has exposed copper (unplated) at the end of the lead terminals due to the manufacturing process. A solder fillet at the exposed copper edge cannot be guaranteed and is not required to ensure a proper bottom solder connection.

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